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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,593	01/22/2002	William L. Duncan	P6800	6958

7590 12/13/2004

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EXAMINER	
CHASE, SHELLY A	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,593	DUNCAN ET AL.	
	Examiner	Art Unit	
	Shelly A Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,7,18,25,27,30 and 31* is/are rejected.

7)☒ Claim(s) *2,4,5,8-10,19-22,26,28,29 and 32-34* is/are objected to.

8)☒ Claim(s) *11-17,23,24 and 35-41* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-1-2002*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *12-6-2004*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 to 10, 18 to 22 and 25 to 26, drawn to error detection, classified in class 714, subclass 763.

   II. Claims 11 to 17, 23 to 24 and 35 to 41, drawn to formatting a storage device, classified in class 711, subclass 170.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention group II has separate utility such as memory configuration. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Tarek Fahmi Reg. No., 41402 on November 12, 2004 a provisional election was made without traverse to prosecute the invention of group I, claims 1 to 10, 18 to 22 and 25 to 34. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11 to 17, 23 to 24 and 35 to 41 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shelly A Chase

DETAILED ACTION

6. Claims 1 to 41 are presented for examination.

Information Disclosure Statement

7. The references listed in the information disclosure statement submitted on 10-01-2002 have been considered by examiner (see attached PTO-1449).

Claim Objections

8. Claims 12 and 34 are objected to because of the following informalities: please change the dependency, for instance, claim 10 should depend on claim 9.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims **1, 3, 7, 18, 25, 27** and **31** are rejected under 35 U.S.C. 102(e) as being anticipated by Hashemi (USPAP 2002/0184556 A1).

Claim **1:**

Hashemi teaches a data storage array with block verification information. The array, comprising: a storage subsystem [400] with storage devices [410] including a plurality of storage blocks storing data in a stripe unit wherein the strip unit includes data blocks ("data field") for storing data and parity blocks ("checksum field") for storing parity data (see par. 0026). Hashemi also teaches that a stripe unit is read for error detection (see par. 0027).

Hashemi further teaches during an initialization phase a logical block address ("pattern") is written to the storage block (see par. 0029-0030). Hashemi teaches that a CRC/LBA generation/check logic [420] checks the CRC to detect errors in the storage block and the logic also checks the LBA data applied to the block by reading the old data and comparing it with the new data (see par. 0033).

Hashemi teaches that a verification process checks the data stored in the respective field with expected data by checking the logical block address and/or the CRC code (see par. 0034-0035). Hashemi further teaches that if a mismatch occurs then a stripe is not initialized ("error") and the storage controller uses the mismatch data to initialize the storage block (see par. 0035).

As per claim **3**, Hashemi teaches that storage controller issues a read request for accessing blocks in the storage devices (see par. 0027).

As per claim **7**, Hashemi discloses that stripe units are read from the storage devices comprising storage blocks A(0) to A(3) and parity block P(A) or storage blocks b(0) to B93) and parity block P(B) (see par. 0027).

Claim **18**:

Hashemi teaches a data storage array with block verification information. The array, comprising: a storage subsystem [400] with storage devices [410] including a plurality of storage blocks storing data in a stripe unit wherein the strip unit includes data blocks ("data field") for storing data and parity blocks ("checksum field") for storing parity data (see par. 0026). Hashemi also teaches that a storage block controller [401] ("means for retrieving") reads a stripe unit for error detection (see par. 0027).

Hashemi further teaches during an initialization phase a logical block address ("pattern") is written to the storage block (see par. 0029-0030). Hashemi teaches that a CRC/LBA generation/check logic [420] ("means for determining whether a checksum") checks the CRC to detect errors in the storage block and the logic also checks the LBA data applied to the block by reading the old data and comparing it with the new data (see par. 0033).

Hashemi teaches that a verification process checks the data stored in the respective field with expected data by checking the logical block address and/or the CRC code using the logic [420] (see par. 0034-0035). Hashemi further teaches that if a mismatch occurs then a stripe is not initialized ("error") and the storage controller uses the mismatch data to initialize the storage block (see par. 0035). Hashemi teaches that the logic checks the CRC and logic block address for mismatch conditions with respect to comparing expected data with data read.

Claim **25**:

Hashemi teaches a data storage array with block verification information. The array, comprising: a storage subsystem [400] with storage devices [410] including a plurality of storage blocks storing data in a stripe unit wherein the strip unit includes data blocks ("data field") for storing data and parity blocks ("checksum field") for storing parity data (see par. 0026). Hashemi also teaches that a stripe unit is read for error detection (see par. 0027).

Hashemi further teaches during an initialization phase a logical block address ("pattern") is written to the storage block (see par. 0029-0030). Hashemi teaches that a CRC/LBA generation/check logic [420] checks the CRC to detect errors in the storage block and the logic also checks the LBA data applied to the block by reading the old data and comparing it with the new data (see par. 0033).

Hashemi teaches that a verification process checks the data stored in the respective field with expected data by checking the logical block address and/or the CRC code (see par. 0034-0035). Hashemi further teaches that if a mismatch occurs then a stripe is not initialized ("error") and the storage controller uses the mismatch data to initialize the storage block (see par. 0035).

As per claim **27**, Hashemi teaches that storage controller issues a read request for accessing blocks in the storage devices (see par. 0027).

As per claim **31**, Hashemi discloses that stripe units are read from the storage devices comprising storage blocks A(0) to A(3) and parity block P(A) or storage blocks b(0) to B93) and parity block P(B) (see par. 0027).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims **6** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi in view of Patterson (USP 6629273).

As per claims **6** and **30**, Hashemi does not specifically teach the checksum is computed with an Exclusive-OR (XOR) operation; however, Patterson in an analogous art teaches detecting errors in a storage subsystem comprising a plurality of storage blocks wherein the parity data is computed via an XOR operation (see col. 3, lines 60 to 64). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the computation of parity data of Hashemi to include computing parity data using XOR operations as taught by Patterson since, Patterson teaches that computing the parity using XOR is a standard in the art. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a know standard to compute parity data

Allowable Subject Matter

13. Claims 2, 4, 5, 8 to 10, 19 to 22, 26, 28 to 29, 32 to 34, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Shelly A Chase